REMARKS

The Office Action dated July 1, 2005, has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

Claims 1, 9 and 17 are amended to more particularly point out and distinctly claim the subject matter of the invention. No new matter is added and no further consideration and/or search is needed. Claims 1-17 are pending in the present application, and are respectfully submitted for consideration.

Claims 1, 2, 4-10 and 12-17 were rejected under 35 U.S.C. § 102(e) as allegedly anticipated by U.S. Patent Application Publication No. US 2004/0174199 (Simon). Further, claims 3 and 11 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Simon. In making the obviousness rejection, the Office Action took the position that Simon taught all the elements of claims 1, 2, 4-10 and 12-17, and that it would have been obvious to use a third order filter for Simon's low pass filter to teach all the elements of claims 3 and 8. The Office Action makes these rejections final. Applicant respectfully traverses the anticipation and obviousness rejections, and respectfully submits that the cited reference fails to disclose or suggest all the features of any of the presently pending claims.

Claim 1, upon which claims 2-8 are dependent, recites a method including receiving an input current from a digital to analog converter. The method also includes mirroring the input current. The method also includes converting the received input

current to a voltage. The method also includes filtering the voltage and converting the filtered voltage into an output current using the mirrored input current.

Claim 9, upon which claims 9-16 are dependent, recites a system including a current mirror that mirrors an input current from a digital to analog converter. The system also includes a first MOSFET capable of converting the received input current to a voltage. The system also includes a filter, communicatively coupled to the first MOSFET, capable of filtering the voltage. The system also includes a second MOSFET, communicatively coupled to the filter and the current mirror, capable of converting the filtered voltage into an output current using the mirrored input current.

Claim 17 recites a system including means for receiving an input current from a digital to analog converter. The system also includes means for mirroring the input current. The system also includes means for converting the received input current to a voltage. The system also includes means for filtering the voltage. The system also includes means for converting the filtered voltage into an output current using the mirrored input current.

As discussed in the specification, examples of the present invention enable generation of an IF output signal amplitude that is substantially less sensitive to process, voltage and temperature than conventional IF output signals. Thus, a new transmitter IF section architecture is provided that experiences less process, voltage and temperature variations. For example, clocking glitches, any quantization noise present, frequency components beyond the cutoff frequency and the like may be filtered out of a signal.

Applicant respectfully submits that the cited reference of Simon fails to disclose or suggest all the features of any of the presently pending claims. Therefore, Simon fails to provide the critical and unobvious advantages discussed above.

Simon relates to a multiplier circuit for the multiplication of two input signals. Referring to Figure 3 of Simon, a multiplier circuit with voltage/current conversion is shown using operational amplifiers for voltage/current conversion and the rest of the circuit with MOS field-effect transistors. In current mirror branches 11 to 14, an RC element, such as a low pass filter, is interposed between input current mirror transistors 11 and 13, and output current mirror transistors 12 and 14. A series resistor 28 and a capacitance 30 are connected downstream of resistor 28 with respect to reference potential terminal 17. Input transistors 28 and 28 form non-inverting inputs. The control input of an input transistor is in each case connected to the non-inverting inputs 26 and 27 of operational amplifiers. Each input transistor is connected by one of its load terminals to the load terminal of transistor 30 or 31 forming the inverting input of the operational amplifier.

A common load terminal node of transistors 28, 30, 27 and 29 on the reference potential side is connected via respective current mirrors 32, 33, 34 and 35 to a respective terminal for feeding in reference currents 36 and 37. The further load terminals of the operational amplifier input transistors 28, 30, 29 and 31 on the supply potential side are connected to one another and to a supply voltage terminal 25. Additional low pass filters

29 and 30 in the current mirrors 11, 12, 13 and 14 lead to a further improvement of the noise properties of the multiplier circuit.

Applicant submits that Simon fails to disclose or suggest all the features of the presently pending claims. For example, applicant submits that Simon fails to disclose or suggest receiving an input current from a digital to analog converter. Simon describes operational amplifiers 20 or 21 giving the input current to transistors 11 or 13. Simon fails to disclose or suggest input current mirror transistor 11 or 13 being coupled directly to a digital to analog converter. Simon fails to disclose or suggest the input current being received from a digital to analog converter.

In contrast, claim 1 recites "receiving an input current from a digital to analog converter." Claim 9 recites "a current mirror that mirrors an input current from a digital to analog converter. Claim 17 recites means for receiving an input current from a digital to analog converter." Applicant respectfully submits that Simon fails to disclose or suggest at least these features of the presently pending claims, as discussed above.

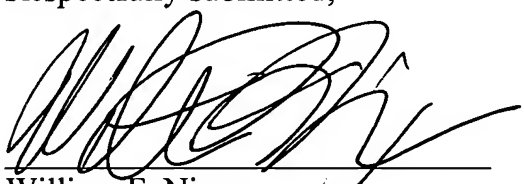
With regard to the dependent claims, applicant submits that they are allowable for the reasons given above, and because the dependent claims recite additional patentable features. Thus, applicant respectfully submits that Simon fails to disclose or suggest all the features of claims 1-17. Applicant respectfully requests that the anticipation and the obviousness rejections be withdrawn.

Applicant further submits that each of claims 1-17 recite subject matter that is neither disclosed nor suggested by the prior art. Applicant therefore respectfully requests that all of claims 1-17 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, applicant respectfully requests that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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